Problem 1

a) Some of the electrical testing was performed at higher-than-normal temperatures or at higher-than-normal voltages. Why would this testing be performed under such stressful conditions even before the chips, boards, or systems have left the manufacturing area?

Soln:- Such testing leads to failure of weak chips, boards, or systems. This prevents further processing of products that are not of the required quality thus saving time and money.

b) How SPM can be used to manipulate single atoms?

Soln: - Scanning probe microscopy (SPM) uses a probe (instead of light source) to image specimen surfaces. This is done by mechanically moving the probe over the surface. And the resolution depends on the size of the probe. Hence, if the probe is sufficiently small it can be used to manipulate single atoms by selectively charging it.

c) List at least three different applications of robotics

Soln: - The following are some of the applications of robotics:-

1. Industrial manufacturing (e.g. welding, assembly, processing)
2. Medicine (e.g. surgical application)
3. Surveillance (e.g. disaster zones, hazardous environments, drones, extraterrestrial bodies)

Problem 2

Consider the diode circuit in figure 1 below. The diodes are both ideal. Determine the voltage at point A, V_A.

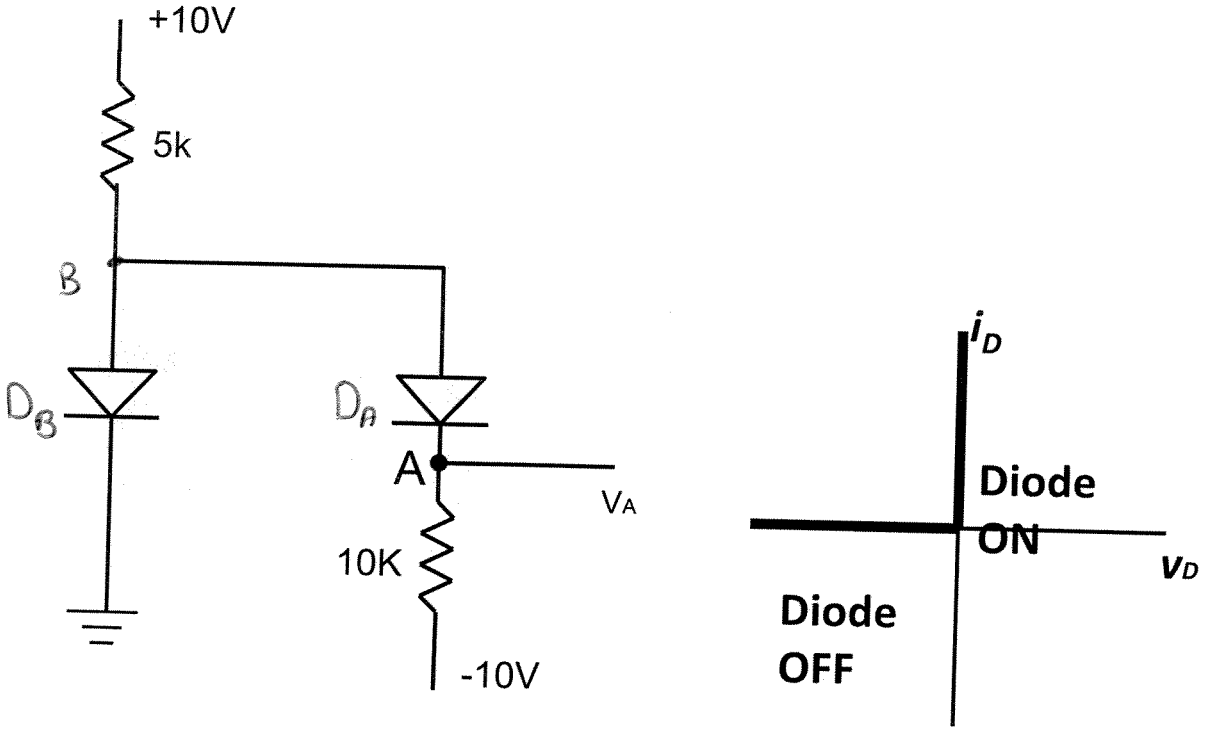


Fig. 1

Diode D_B is turned ON, hence voltage at point B, $V_B = 0$

Similarly diode D_A is turned ON, hence voltage at point A, $V_A = V_B = 0\,V$

Problem 3

In the circuit shown in Fig. 2, assume that both transistors are operating in active region. Find the collector currents I_{C1}, I_{C2}, and the collector to emitter voltages V_{CE1}, V_{CE2} for both transistors if $V_{BE1} = V_{BE2} = 0.7V$ and $\beta_1 = \beta_2 = 50$.

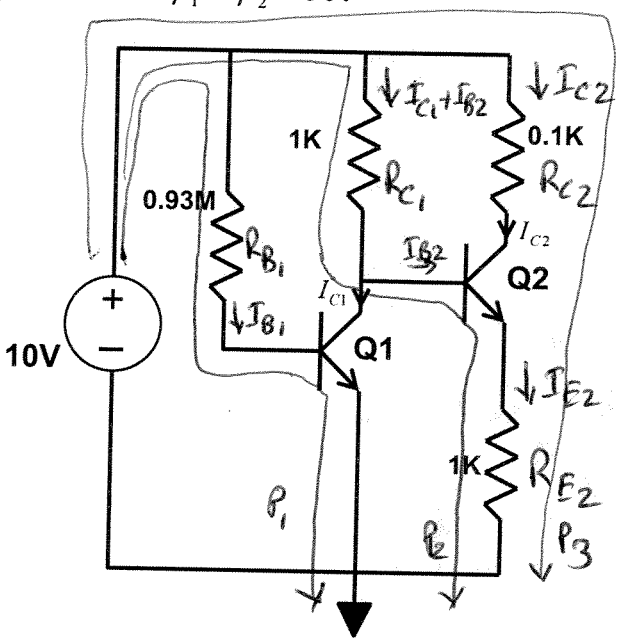


Fig. 2

Applying KVL along P_1

$$-10 + I_{B1} \times R_{B1} + V_{BE1} = 0$$

$$I_{B1} = \frac{10 - 0.7}{930 \times 10^3} = 10\,\mu A$$

$$I_{C1} = \beta \times I_{B1} = 500\,\mu A$$

Applying KVL along P_2

$$-10 + (I_{C1} + I_{B2})R_{C1} + V_{BE2} + I_{E2} \times R_{E2} = 0$$

$$-10 + 0.5 + 0.7 + I_{B2} \times R_{C1} + (\beta+1) I_{B2} \times R_{E2} = 0$$

$$I_{B2}(R_{C1} + 51 \times R_{E2}) = 8.8$$

$$I_{B2} = 169.2\,\mu A$$

$$I_{C2} = \beta \times I_{B2} = 8.5\,mA$$

$I_C = \beta I_B$ & $I_C = \left(\frac{\beta}{\beta+1}\right) I_E$

$I_E = (\beta+1) I_B$

$$V_{C1} = 10 - (I_{C1} + I_{B2}) * R_{C1}$$

$$V_{C1} = 10 - (500 + 169.2)\times 10^{-6} * R_{C1}$$

$$V_{C1} = 9.33\ V$$

$$V_{CE1} = V_{C1} = \underline{9.33\ V}$$

Applying KVL along P_3

Note: $I_{E2} = I_{C2} + I_{B2} = 8.669\ mA$

$$-10 + I_{C2} * R_{C2} + V_{CE2} + I_{E2} * R_{E2} = 0$$

$$-10 + 0.85 + V_{CE2} + 8.669 = 0$$

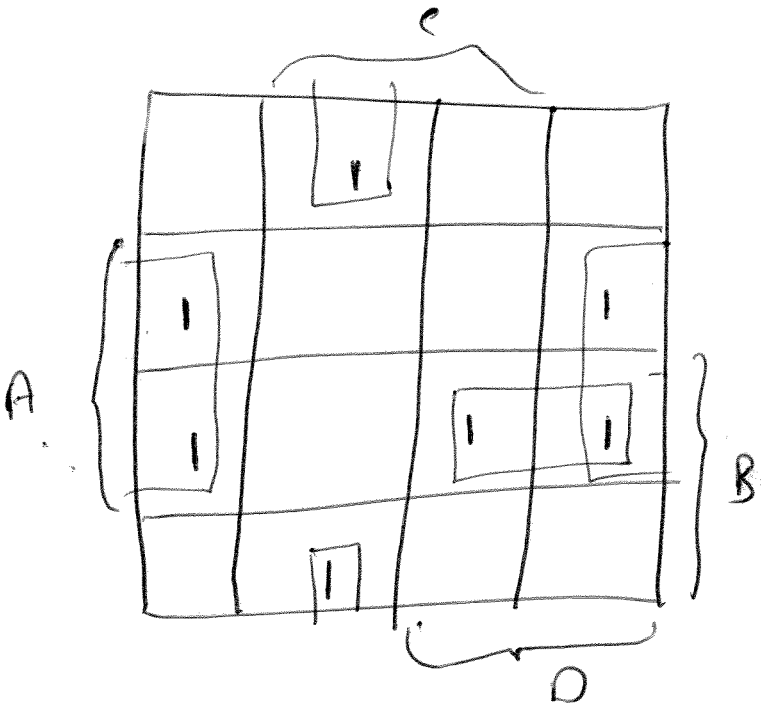
$$V_{CE2} = 0.481\ V$$

Problem 4

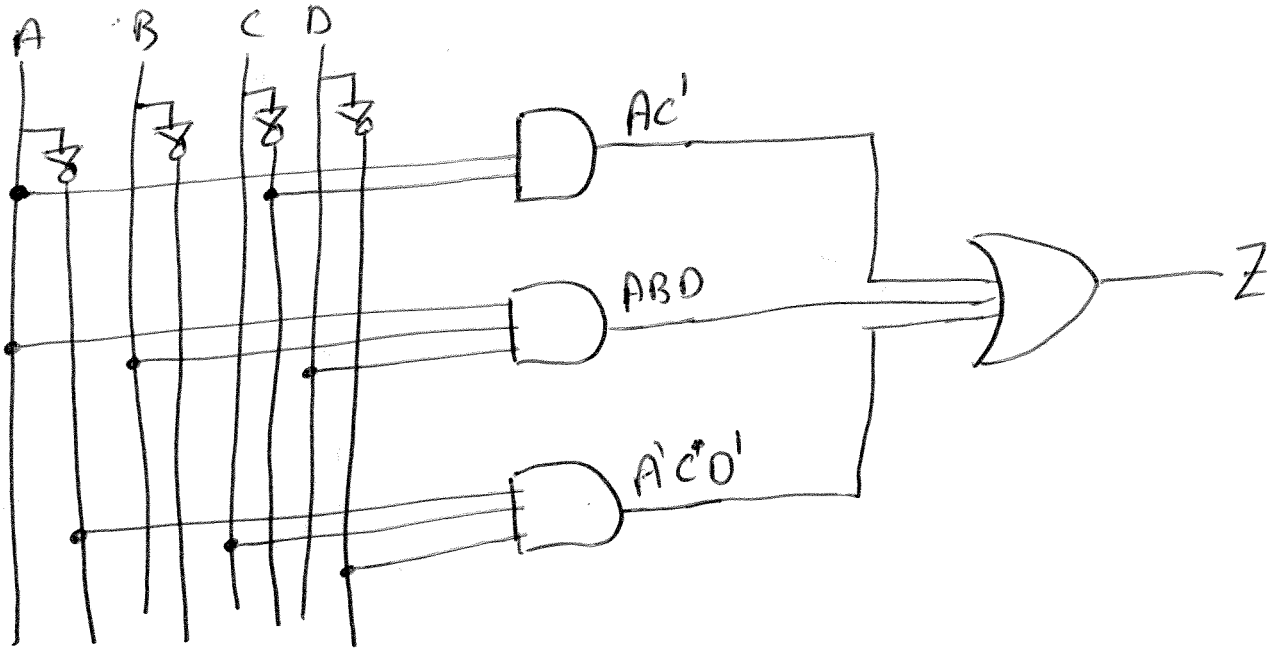
a) Use Karnaugh map to obtain the minimum SOP (sum of product) form for the following Boolean function:

Z = ABC'D' + AB'C'D' + ABC'D + AB'C'D + ABCD + A'B'CD' + A'BCD'

b) Then implement the minimum SOP expression using logic gates.

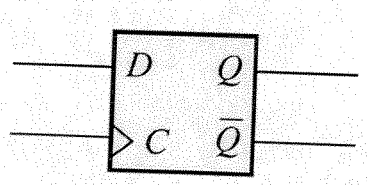


SOP => $AC' + ABD + A'CD'$



Problem 5

The input D to a positive-edge triggered flip-flop is shown in figure 3 below. Find the output signal Q



(a) Circuit symbol

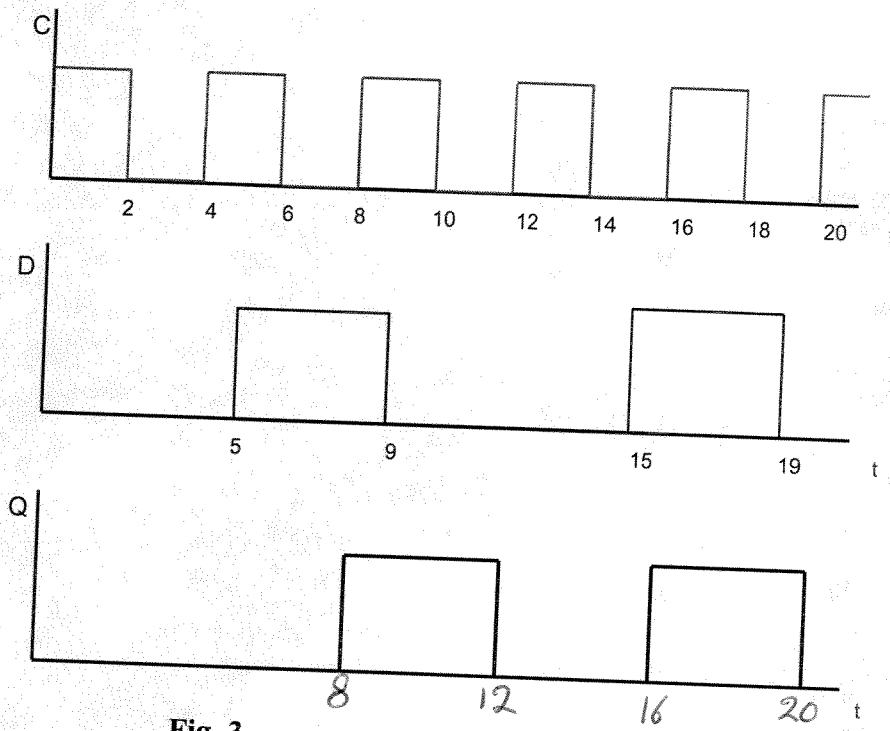


Fig. 3